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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,429	11/03/2003	Glenn Joseph Leedy	ELM-1 Cont. 10	5639

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/700,429	LEEDY, GLENN JOSEPH	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *77-272* is/are pending in the application.

4a) Of the above claim(s) *77-109,211-222 and 254-272* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *110-209 and 223-258* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08). Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on October 05, 2006 has been entered and forwarded to the Examiner on October 18, 2006.

Therefore claims 109, 122,135,163,179 and 195 as amended by the amendment and claims 110-121,123-134, 136-162, 164-178, 180-194, 196-210 and 223-258 as previously recited are currently pending in the application.

Claims 77-108, 211-222 and 259-272 are currently withdrawn from consideration.

Claims 1-76 were previously cancelled.

Information Disclosure Statement

No further IDSs after the one filed on January 11, 2006 has been filed in this case.

Claim Rejections - 35 USC Section 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains

Patentability shall not be negatived by the manner in which the invention was made.

Claims 109-201 and 223-258 are rejected under 35 U.S.C. 103 as being unpatentable over Shimoji (U.S. Patent No. 5,420,458, herein after Shimoji) and Mattox (U.S. Patent No. 4,825,277, herein after Mattox).

With respect to claim 109, 122,163, 179 and 195, Shimoji describes a method of making an integrated circuit including the steps of : Forming a thin substrate (Shimoji, Fig. 3 A # 21, col. 3 line 48) and forming on the substrate circuitry including active devices (Shimoji, Fig. 2 C # 51, 52, col. 3 lines 65-68) ;

Shimoji does not specifically describe the integrated circuit is substantially flexible while retaining its Structural integrity.

However Mattox in col. 9 lines 1-13 describes the integrated circuit is ;substantially flexible while retaining its structural integrity to the semiconductor surface.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the Mattox's stress controlled dielectric membrane instead of Shimoji's to dielectric layer form devices having controlled stress relative to the semiconductor surface (Mattox col. 2 lines 5-10).

And removing a major portion of the semiconductor substrate while retaining the structural integrity (Shimoji Fig. 6 B # 8, col. 4 lines 50-57).

With respect to dependent claims110- 114, 123-127, 136-140, 147-150, 153-155, 159-160,164-166,174-176,180-182,190-192, 196-198 and 206-209, wherein the thin substrate is formed prior to forming circuitry (Shimoji, Fig. 3 A # 21, col. 3 line 48)., after forming said circuitry, (Shimoji fig. 4, col. 4 lines 5-15) an elastic dielectric layer overlying the active devices. (Shimoji, Fig. 2 C # 51, 52, col. 3 lines 65-68, Mattox) ; deposition of elastic dielectric film by RF, CVD, PECVD (Mattox, also all well known in the art methods of deposition and also Shimoji col. 4 lines 15-20).

With respect to dependent claims 115, 128, 141,151,156,161,167,177, 183~ 193, 8 2 and 199, wherein the dielectric membrane is caused to have a stress of 8 x 10 dynes/cm or less. (See Mattox claim 9)

Mattox does not specifically mention a surface stress of 8 X 10 8 dynes/cm 2. However Mattox in col. 7 lines 45-52 describes the stress range to be between -1 to 5 x I0 8 g dynes/cms to 1 x 109 to form devices having controlled stress relative to the semiconductor surface .

Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the stress range 8 X 10 8 dynes/cm 2 instead of Mattox's 9 dynes/cms to 1 X 10 9 dynes/cm previously described overlapping range of 1 to 5 X 10 y 2 to form devices having controlled stress relative to the semiconductor surface (Mattox col. 2 lines 5-10).

With respect to claims 116, 119 -120, 129, 132-133, 142, 145-146, 149, 157-159 162-164-165, 168, 171-172,174, 178, 184,187-188, 194, 196-197, 200, 203-204, 206-207 and 210 wherein the stress is tensile (Mattox abstract line 8, etc., silicon or dielectric substrate (Shmioji see rejection of clam 110 above) ;

With respect to remaining claims including claims117-118, 130-131,134-135,141,143-144,145,156,167-170,177,183,185-186,193,195,199 201-202, 206-209 and Claims 121,147 and 205 wherein the integrated circuit can be thinned to 50 microns. (Mattox col. 4 lines'15-23), and 205 wherein .the dielectric layer is formed of inorganic material of an oxide of silicon, a nitride of silicon (Shmioji, silicon dioxide/nitride) or organic (Shmioji or well Know - e.g. TOES).

Response to Arguments

Applicant's arguments filed on Jan. 20, 2006 have been fully considered but they are not persuasive, for the following reasons :

Applicants' arguments with regard to claims 179-194 and 247-252 are based impermissible piece meal analysis of why Shimoji or Mattox individually and not as combined allegedly do not teach/describe the recited " wherein the integrated circuit is elastic while retaining its structural integrity" is not persuasive.

In response to Applicants' piece meal analysis of the references , it has been held that one cannot show non-obviousness by attacking references individually where, as here , the rejections are based on combinations of references .

Applicants' contention that Mattox in col. 9 lines 1-13 does not show or suggest that the integrated circuit is elastic (is recited in claims 195 and 196-210 and 253-258 only , rest of the claims only recite an elastic dielectric – described in Shimoji fig.2 and col. 3 lines 65-68)) is not persuasive because , Mattox col. 9 lines 1-13 states :"

35 As will be appreciated by those of skill in the art based on the description herein, the amount of stress relative to silicon may be adjusted by varying the oxy-nitride mixture composition. This may be done in a more precise way than by use of layered structures as 40 have been used in the past. Further, different portions of the mixture may be tailored to have different compositions and therefore different stresses, smoothly varying therebetween. This cannot be accomplished with prior art arrangements. Further, by using very conformal 45 layers, trapped voids may be eliminated.

35 As will be appreciated by those of skill in the art based on the description herein, the amount of stress relative to silicon may be adjusted by varying the oxy-nitride mixture composition. This may be done in a more precise way than by use of layered structures as 40 have been used in the past. Further, different portions of the mixture may be tailored to have different compositions and therefore different stresses, smoothly varying therebetween. This cannot be accomplished with prior art arrangements. Further, by using very conformal 45 layers, trapped voids may be eliminated.

Accordingly, it has been found that it is more desirable to operate in a composition range slightly biased toward tensile stress in the oxy-nitride so as to insure 5 that there is little or no compressive stress in the nitride (and tensile stress in the semiconductor) and limited tensile stress in the nitride (and compressive stress in the semiconductor) over the expected temperature range. Thus, the compositional ranges which accomplish this 10 are preferred. That the proper composition has been obtained may be conveniently determined from the refractive index.

it is noted from the above that Mattox teaches that the substrate (including the integrated circuit) has different stress (e.g. tensile or compressive) and (not only the oxynitride plugs 58 as stated by Applicants' , but the complete reading of Mattox must include the substrate also) and the substrate do not break and unless they are elastic,

they will develop cracks or break when subjected to stress and render the device inoperable.

Applicants' contention is that the applied (Shimoji or Mattox) references do not describe/suggest making an integrated circuit "wherein the integrated circuit is elastic while retaining its structural integrity" is not persuasive because Shimoji Fig. 6 B # 8, col. 4 lines 50-57 (as stated in the rejection above), and also col. 5 lines 1-5 and lines 27-29 (reproduced below)

> And still further, the present invention does not allow the silicon substrate to be formed thin throughout, but partly forms the bottom recessed parts 8 so as to leave 2: the unetched N+ type silicon substrate 21 except for the bottom recessed parts 8. The resulting semiconductor device, therefore, has a sufficient strength and an excellent durability.

show that applicants' arguments are based on perhaps an incomplete reading of the applied references and a complete reading shows the applied references showing teachings of making an integrated circuit "wherein the integrated circuit is elastic while retaining its structural integrity.

Shimoji"s col. 5 lines 27-29 describe removing a portion of the bottom surface of the substrate (which is a part of the integrated circuit) and thereby forming the resulting semiconductor device (included in the I/C) has sufficient strength and excellent durability similar to Applicants' recitation of wherein the integrated circuit is elastic while retaining its structural integrity similar to wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

Applicants' essentially repeat the same arguments with respect to claim dependent claims 110-121, 148-152, 222-228 dependent upon claim 109; claims 123-134, 153-157 and 229-234 dependent upon claim 122; claims 136-147,158-162 and 235-240 dependent upon claim 135 ; claims 164-178 and 241-246 dependent upon claim 163 and claims 196-210 and 253-258 dependent upon claim 195, namely the applied references to show/describe "wherein the integrated circuit is elastic while retaining its structural integrity" is not persuasive for reasons set out above and incorporated here by reference for sake of brevity.

Therefore all of applicants' arguments are not found to be persuasive and all the pending claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven H. Rao

Patent Examiner

December 21, 2006.